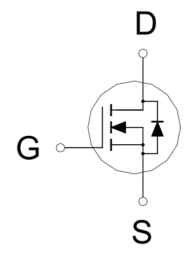
NIKO-SEM

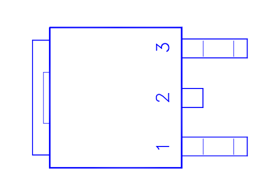
N-Channel Logic Level Enhancement Mode Field Effect Transistor

P3056LD
TO-252 (DPAK)

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
25	50mΩ	12A





1. GATE
2. DRAIN
3. SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_C = 25 °C	I_D	12	A
	T_C = 100 °C		8	
Pulsed Drain Current[1]		I_{DM}	45	
Avalanche Energy	L = 0.1mH	E_{AS}	60	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	3	
Power Dissipation	T_C = 25 °C	P_D	48	W
	T_C = 100 °C		20	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	275	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		3	°C / W
Junction-to-Ambient	$R_{\theta JA}$		75	
Case-to-Heatsink	$R_{\theta CS}$	1		

[1]Pulse width limited by maximum junction temperature.
[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250µA	25			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250µA	0.5	0.7	1.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±250	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V			25	µA
		V_{DS} = 20V, V_{GS} = 0V, T_J = 125 °C			250	

On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	12			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 5V, I_D = 12A		70	120	mΩ
		V_{GS} = 10V, I_D = 12A		50	90	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15V, I_D = 12A		16		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		450		pF
Output Capacitance	C_{oss}			200		
Reverse Transfer Capacitance	C_{rss}			60		
Total Gate Charge[2]	Q_g	V_{DS} = 0.5$V_{(BR)DSS}$, V_{GS} = 10V, I_D = 6A		15		nC
Gate-Source Charge[2]	Q_{gs}			2.0		
Gate-Drain Charge[2]	Q_{gd}			7.0		
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DS} = 15V, R_L = 1Ω, I_D ≅ 12A, V_{GS} = 10V, R_{GS} = 2.5Ω		6.0		nS
Rise Time[2]	t_r			6.0		
Turn-Off Delay Time[2]	$t_{d(off)}$			20		
Fall Time[2]	t_f			5.0		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				12	A
Pulsed Current[3]	I_{SM}				20	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.5	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100A / µS		30		nS
Peak Reverse Recovery Current	$I_{RM(REC)}$			15		A
Reverse Recovery Charge	Q_{rr}			0.043		µC

[1]Pulse test : Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

REMARK: THE PRODUCT MARKED WITH "P3056LD", DATE CODE or LOT #

TO-252 (DPAK) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	9.35		10.10	H		0.80	
B	2.20		2.40	I	6.40		6.60
C	0.45		0.87	J	5.00		5.50
D	0.89		1.50	K	0.55		1.10
E	0.45		0.60	L	0.60		1.00
F	0.03		0.23	M	4.40		4.60
G	5.35		5.65	N			

